Au2001: Position (Non-Magnetic) Sensor for Water & Gas AMR/AMI

General Description

Au2001 is a position sensor IC targeted for water & gas metering applications. It covers a range of working distance required in water & gas meters. The IC supports SPI for simple interface with micro controllers. The IC works on a wide range of supply from 2.4 V-3.6 V. The IC supports two modes – low sensitivity mode for lesser sensing distance and high sensitivity mode for larger sensing distance. The average current is less than 0.6 uA in low sensitivity mode and less than 4.5 uA in high sensitivity mode, when triggered once in 125 ms.

The IC is available in 3 mm x 3 mm 16 pin QFN package.

Features

- Ultra-low power consumption
- Operation Temperature Range of -20 °C to 70 °C
- 3 mm × 3 mm, 16-Pin QFN package

Applications

- Water & Gas Flow Metering
- Product Counting in production line

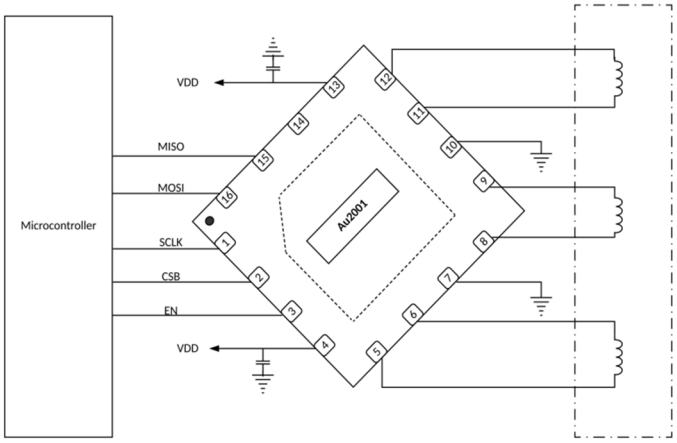

Figure 1 Typical Application Schematic

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1 Pin Configuration

Au2001 is a sensor IC to detect the rotation of a metal plate. This is specifically targeted for non-magnetic water & gas flow meters.

1.1 Pin Configuration Diagram

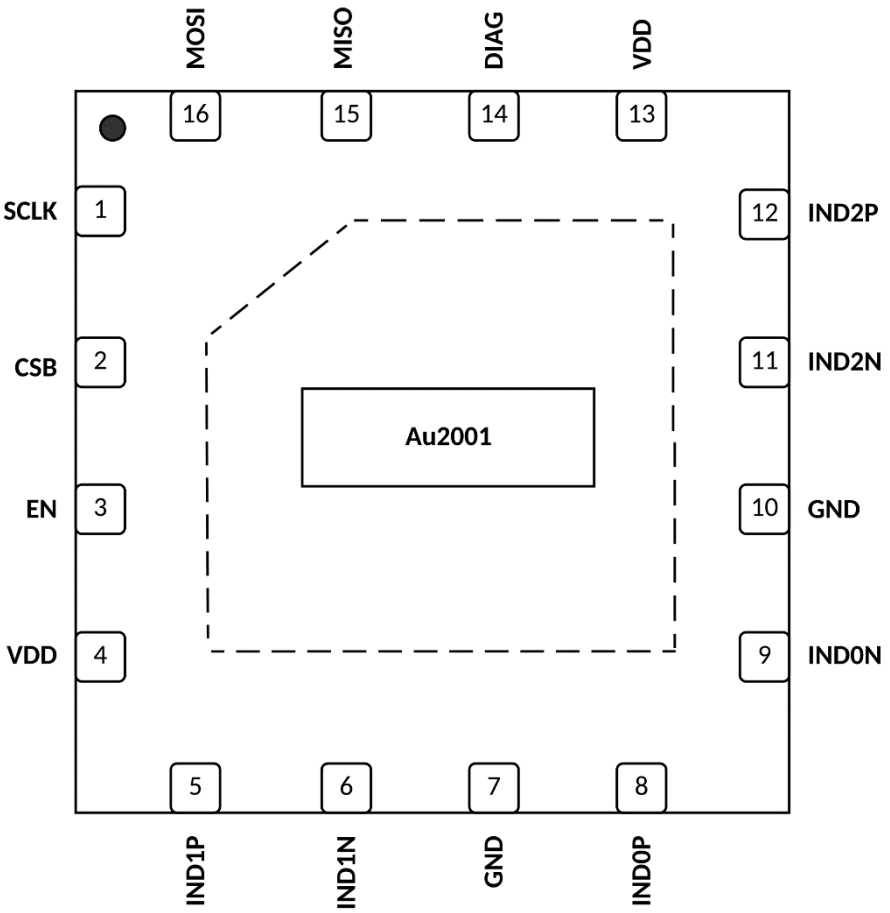


Figure 2 Au2001 Pin Configuration

1.2 Pin Description

Table 1 Pin Functions

Pin No.	Pin Name	Description
5	IND1P	P-terminal of PCB coil 1
6	IND1N	N-terminal of PCB coil 1
12	IND2P	P-terminal of PCB coil 2
11	IND2N	N-terminal of PCB coil 2
8	IND0P	P-terminal of PCB coil 0
9	IND0N	N-terminal of PCB coil 0
4,13	VDD	Supply
7,10	GND	Ground
3	EN	Enable the Sensor
1	SCLK	Clock for SPI interface
16	MOSI	SPI-Master Out Slave In
15	MISO	SPI-Master In Slave Out

Pin No.	Pin Name	Description
2	CSB	Slave Select – Active Low
14	DIAG	Diagnostic pad for measuring any of the internal voltages for debug purposes

2 Electrical Specifications

Table 2 Absolute Maximum Ratings

Parameter	Conditions	Symbols	Min	Typ	Max	Units
Line Supply Voltage	V_{LINE}		-0.3		3.9	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 4. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 3 Recommended Operating Conditions

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Line Supply Voltage	VDD		2.4		3.6	V
Temperature	Operation temperature		-20		70	°C

Table 4 ESD Ratings

Parameter	Conditions	Symbols	Min	Typ	Max	Units
Human Body Model		HBM		4000		V
Charged Device Model		CDM		500		V
Latch Up		LU		200		mA

3 Power Consumption in Different Modes

The following is the typical power consumption in the different radio modes

Table 5 Power Consumption in Different Modes

All typical values at +25 °C

IC Mode	Supply	Current Consumption (typ)	Unit
Idle	V_{LINE} = 3.6 V	0.1	uA
Average current consumption in low sensitivity mode*	V_{LINE} = 3.6 V	0.6	uA
Average current consumption in high sensitivity mode*	V_{LINE} = 3.6 V	4.5	uA

Notes: *-Measured when the sensor is triggered once in 125 ms

4 Interface with Microcontroller

Micro controller can interface with Au2001 using a simple SPI

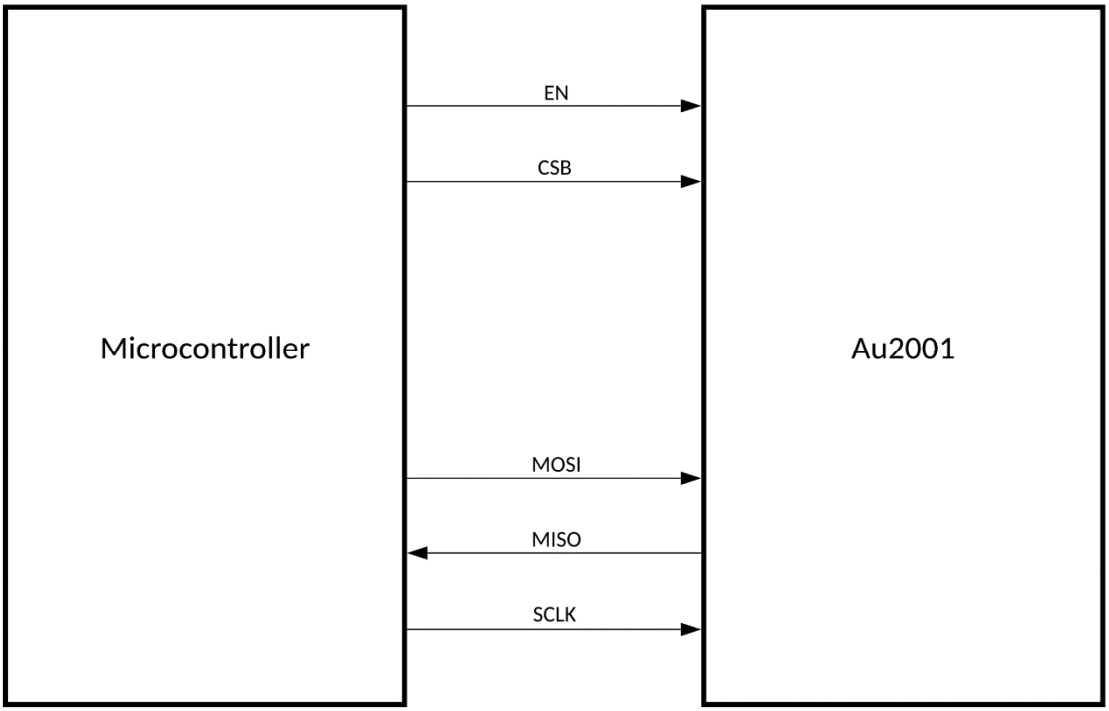


Figure 3 Microcontroller Interface

4.1 Timing sequence of a measurement cycle

4.1.1 Initial Sequence

When the sensor powers up for the first time, the microcontroller has to give a reset command to the sensor to reset the IC to a known initial state.

4.1.2 Measurement Sequence

There is a certain sequence of events that needs to be followed by the microcontroller to detect the presence of metal plate. The sequence of events is summarized in Figure 4.

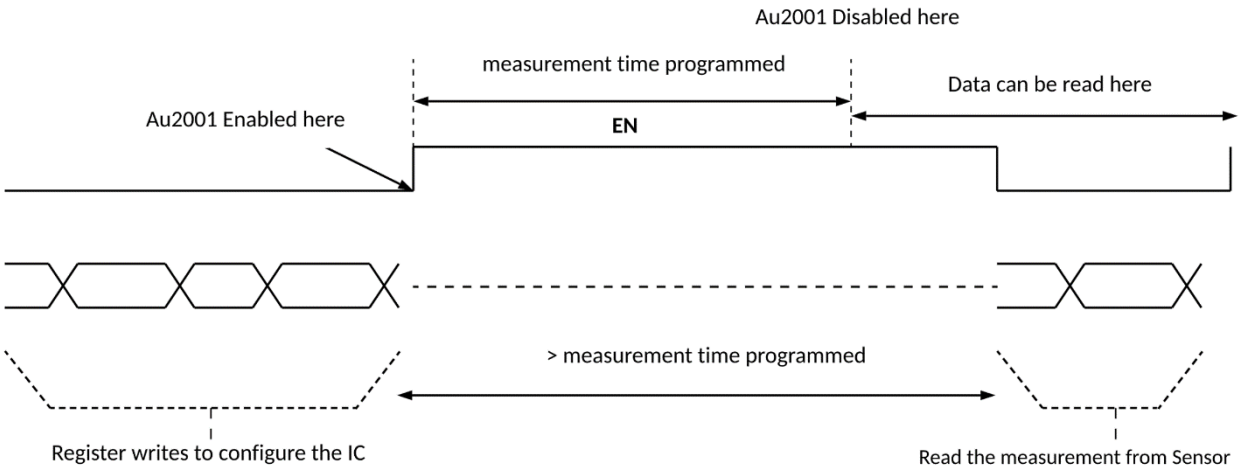


Figure 4 Measurement Sequence

The above measurement sequence can be split-up into 3 sections

- **Configuration:** The microcontroller sets the measurement time parameter in Au2001 using register write.
- **Measurement:** To trigger the measurement, EN is asserted. EN has to be held high for a minimum duration of programmed measurement time mentioned in configuration and an additional time of 10 us. Valid bit in the register map is asserted once the measurement is done. This can be polled to de-assert the EN signal. Once the measurement is done and the corresponding data is written to the registers, Au2001 is powered down automatically. Hence there is no limit on the maximum time for which EN can to be held high. EN signal should be de-asserted and asserted again before the next measurement.
- **Data Read Back:** The data regarding the presence of metal plate can be read any time after the minimum duration. Data valid bit in the register indicates the validity of the data read. The data will be valid till the next measurement cycle is triggered by assertion of EN signal.

4.2 Serial Peripheral Interface

The Serial Peripheral Interface (SPI) in Au2001 is a slave only interface and supports both the conventional register access as well as short commands. To talk to the slave, the SPI master in the microcontroller has to be configured in the modes: clock polarity (CPOL) = 1 and clock phase (CPHA) = 1 or clock polarity (CPOL) = 0 and clock phase (CPHA) = 0. The data sent and received is aligned to the byte boundary.

4.2.1 Interface Signals

The Slave uses a four-wire serial interface. The signals in the interface are described below

Table 6 Interface Signals

Signal Name	Direction	Description
MOSI	Input	SPI Master-Out-Slave-In (MOSI) signal
MISO	Output	SPI Master-In-Slave-Out (MISO) signal
SCLK	Input	SPI serial clock. The entire slave runs on this clock
CSB	Input	SPI chip select. The signal has an active-low polarity

All control and data signals in the interface are assumed to be synchronous to the serial clock, sclk.

4.2.2 Serial Interface Timing at Bit-Level

A transaction is initiated by asserting the chip-select, csb (low), clocking the serial clock line (sclk) and driving the input data to the chip on mosi and sampling the output data from the chip on miso. The data is shifted in little-endian format (MSB first), at bit level. The data sent or received must be aligned to the byte boundary. When csb is de-asserted, by default, the slave will leave the miso line floating. The bit-level timing can comply with two SPI modes, as shown in Figure 5 and Figure 6

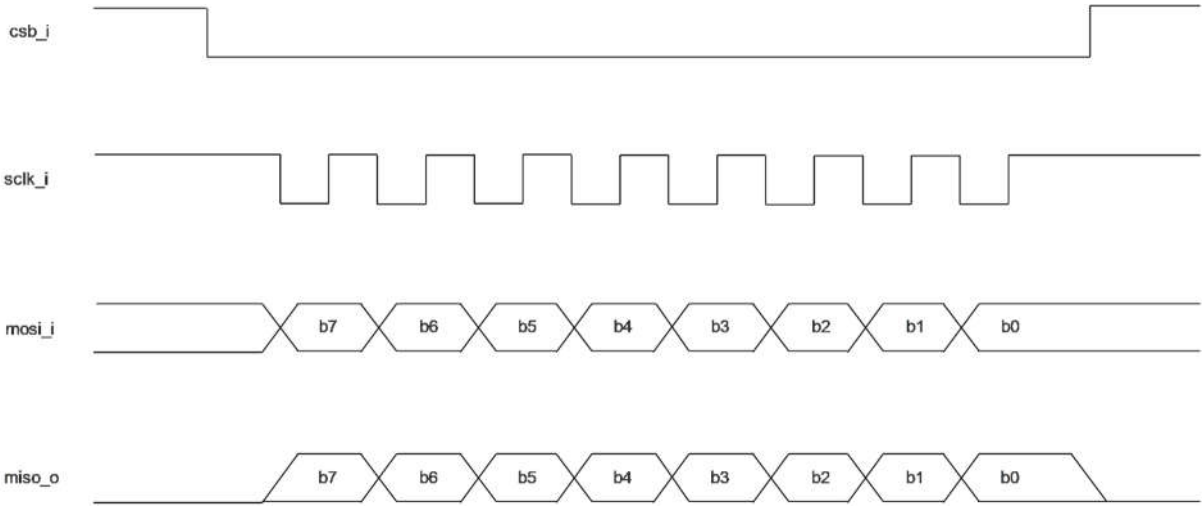


Figure 5 SPI timing for mode CPHA = 1 and CPOL = 1

In mode CPHA = 1 and CPOL = 1, the state of the clock line when csb is high is high. Both the master and slave drive data during the falling edge of sclk and sample data during the rising edge of sclk. Another SPI mode that is supported is mode CPHA = 0 and CPOL = 0. The bit-level timing for this mode is given in Figure 6

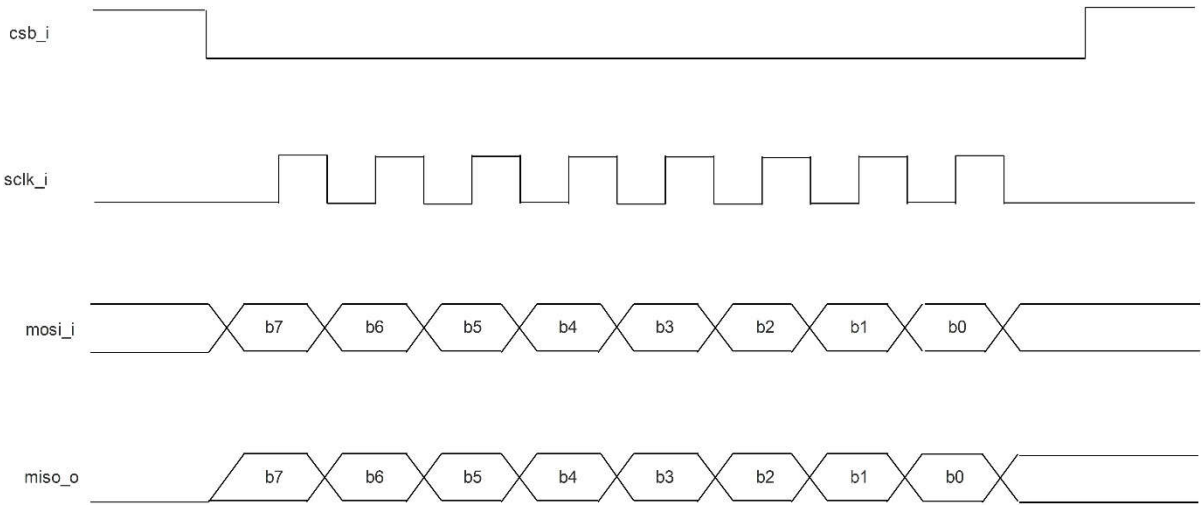


Figure 6 SPI timing for mode CPHA = 0 and CPOL = 0

In mode CPHA = 0 and CPOL = 0, the state of the clock line when csb is high is low. Both the master and slave drive data during the falling edge of sclk and sample data during the rising edge of sclk. As shown in the timing diagram, the MSB of the data has to be set-up before the first rising edge of sclk.

Since data is aligned to the byte boundary and given these timing specifications, the bit level timing information relative to sclk will be omitted from most of the subsequent figures, unless it is absolutely necessary.

4.2.3 Naming Conventions used while describing SPI

This section covers a few terms that are used while describing the SPI interface, in the rest of the document.

4.2.3.1 Transaction

An SPI transaction consists of a complete cycle where the csb is asserted, one or more bytes are sent and received and csb is de-asserted.

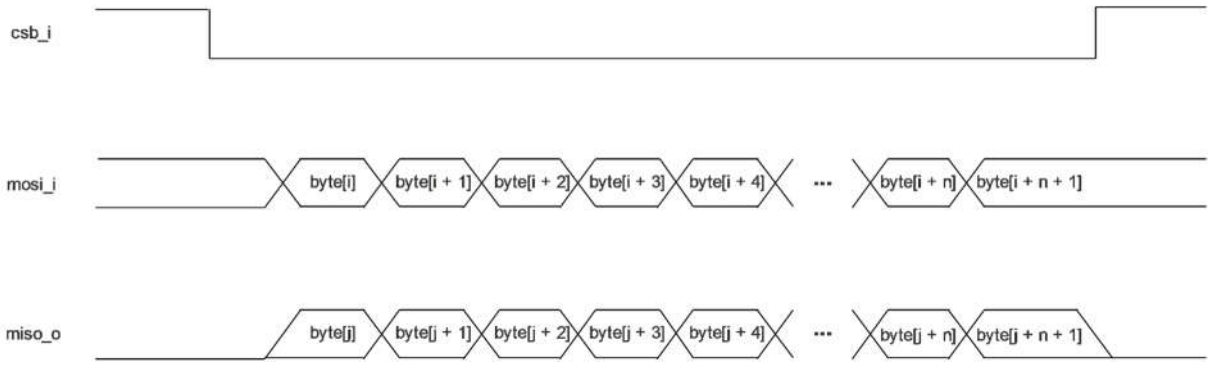


Figure 7 An SPI transaction, interpreted at byte level

4.2.3.2 Frame

One or more bytes sent during a transaction, may be a part of a larger word which is called a frame. The length of the frame in bytes is determined by a header, which is described in detail in the next section. A frame boundary is always referred with respect to the data sent by the master. A frame cannot spread across two transactions.

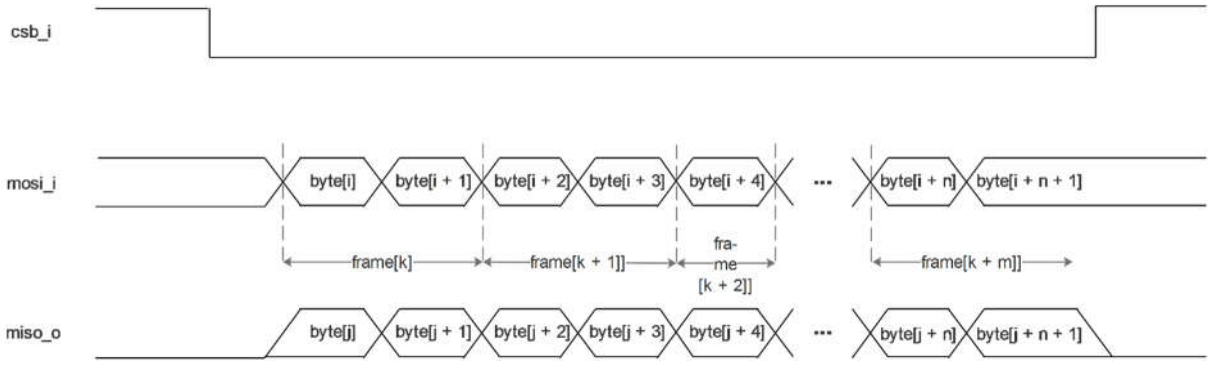


Figure 8 An SPI transaction, interpreted at frame level

4.2.3.3 Command and Arguments

Every frame sent by the master begins with a two-bit header called a command. The command decides the frame length and frame format. Additional bits in the frame may constitute arguments to the command, as prescribed by the frame format. The last argument may be padded with zeros on the LSB side, to align the frame to the byte boundary.

Table 7 Generic Frame Format

Command (2 bits)	Argument 1	Argument 2	…	Argument n	Zero-padding (optional)

4.2.3.4 Data from slave and address pointer

While the master can send frames of different lengths to the slave, which specify different commands, the data sent by the slave is always the data at a particular address in the register map in the slave. The slave has 64 configuration and control registers, each one byte long. Every byte sent by the slave is the data at one of these registers. An internal address pointer decides the register whose data will be sent by the slave, when the next byte is being transferred over SPI from the slave to the master. The address pointer gets updated during or after a frame in sent by the master.

4.2.3.5 SPI Commands

This section describes various commands supported by the slave and the associated frame formats. The commands are summarized in the table below and described in detail in the subsequent sections.

Table 8 SPI Commands

Command	Header code	Description
Reset	0x03	Resets all configuration and control registers to their defaults.
Write register	0x01	Writes to a register in the register map
NOP/Read register	0x00	No action taken/Reads from a register in the register map

Many commands accept a register address as their argument. This address is copied to the internal address pointer in the slave. The first byte sent by the slave during the next frame is the data at this address. If the frame is longer than one byte, the data sent by the slave during other bytes in the frame is specified in the frame format.

4.2.3.6 Reset

This command resets the configuration registers in the register map and all other control registers in the chip. The reset command frame is one byte long. This command accepts the address of the register to be read during the next transaction as an argument.

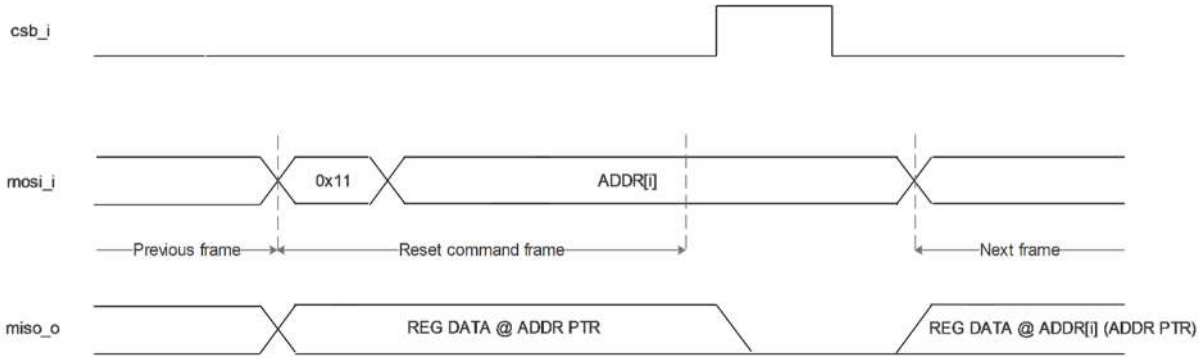


Figure 9 Reset Command Frame

4.2.3.7 Write Register

The write register command frame is two bytes long and performs write to a configuration register in the slave. The command accepts the address of the register to be written and the data to be written to the register as arguments.

Table 9 Write Command Frame Format

15 : 14	13 : 8	7 : 0
0x01	Address of register to be written	Data to be written to the register

The timing diagram for this frame is given below (No waveform attached)

During the first byte of this frame, the slave sends the data at the register address stored in the internal address pointer. At the same time, the address of the register to be written, as specified by the master, is copied to the address pointer. During the second byte of this frame, the slave sends the data at the address to be written, specified by the master (old data). At the same time, the data to be written, as specified by the master, is copied to the register. During the next frame, the first byte sent by the slave is the new data at this address.

4.2.3.8 No operation (NOP)/Read register

The NOP command frame is one byte long and causes the slave to take no action. The command accepts the register to be read during the next frame as an argument. The address is copied to the internal address pointer. The frame format is given in Figure 10

Table 10 NOP/Read Command Format

7 : 6	5 : 0
0x00	Register to be read during the next frame

The timing diagram for this frame is given below

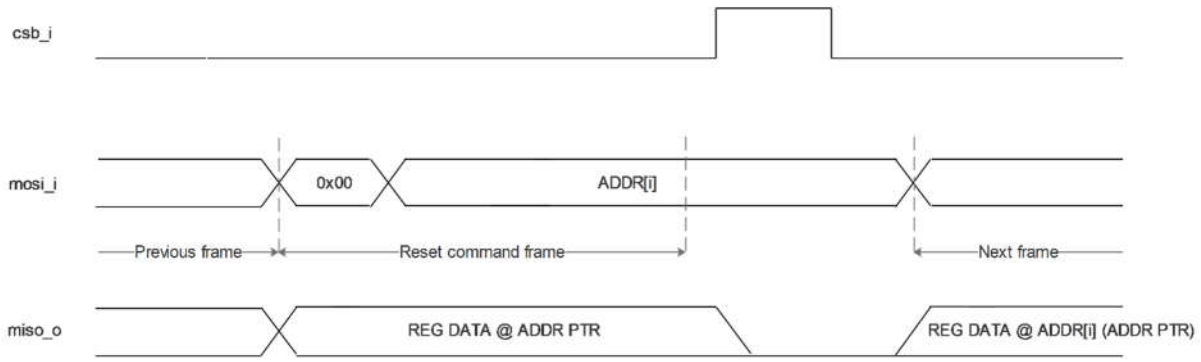


Figure 10 NOP/Read Command Format

5 Application Diagrams

5.1 Interface with Microcontroller and Coil

The Figure 11 shows the normal use case where Au2001 is used as a sensor interfacing with 3 PCB coil and microcontroller

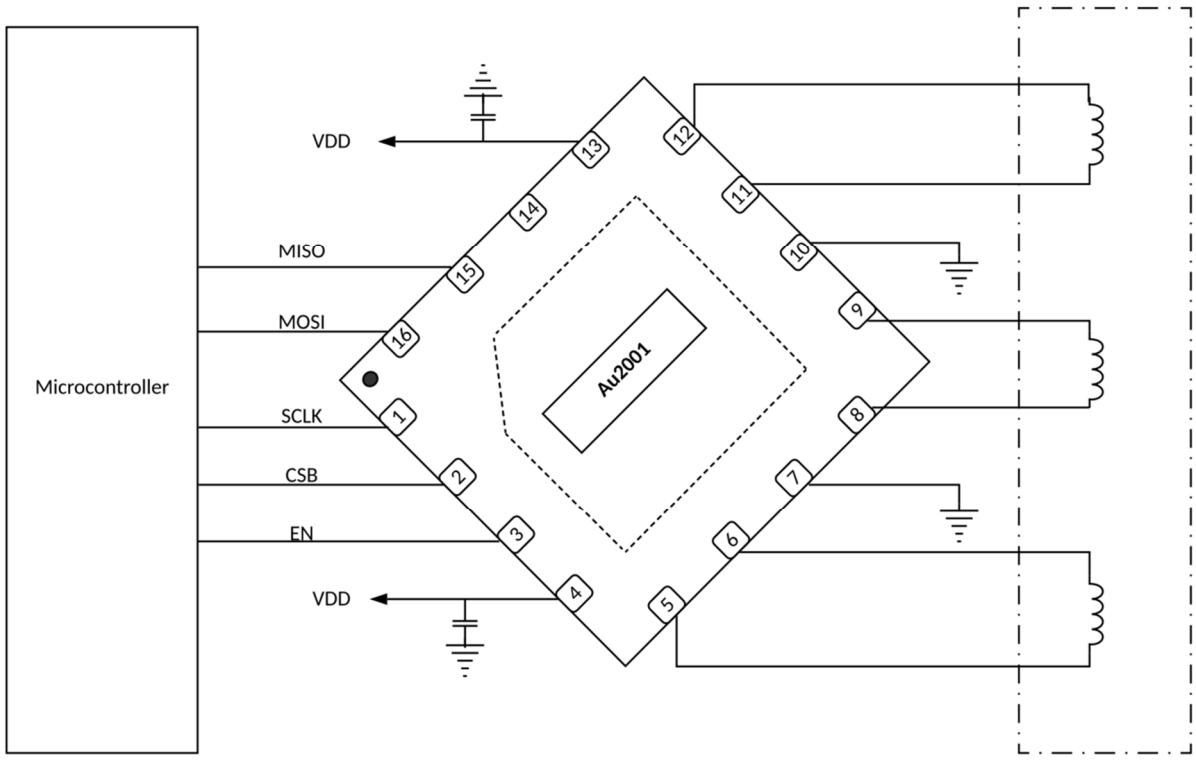


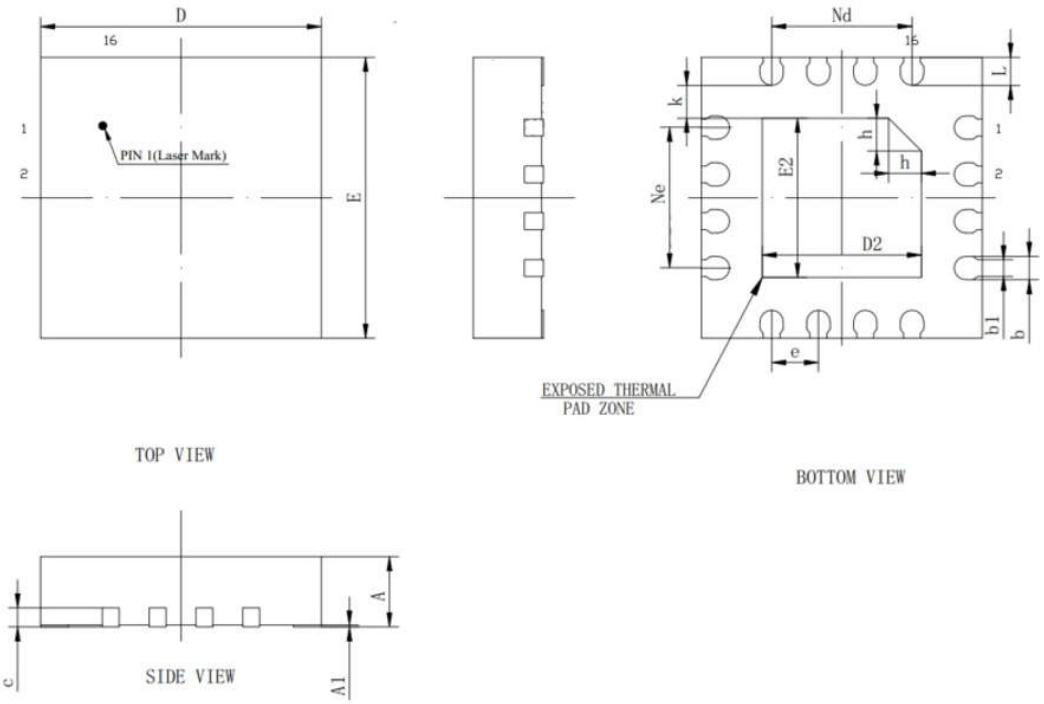
Figure 11 Application Schematic

6 PCB Coil Layout Guidelines

The following layout guidelines should be followed for getting performance

- The WM IC should be placed in the center of the coil. The PCB coil traces can either be on the same plane or the opposite plan.
- The outer loop of the coil should be dictated by the size of the metal plate

7 Package Information



SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.85	0.90	0.95	△
A1	0	0.02	0.05	
b	0.20	0.25	0.30	
b1	0.18REF			
c	0.203REF			
D	2.90	3.00	3.10	
D2	1.60	1.70	1.80	
e	0.50BSC			
Ne	1.50BSC			
Nd	1.50BSC			
E	2.90	3.00	3.10	
E2	1.60	1.70	1.80	
L	0.25	0.30	0.35	
h	0.30	0.35	0.40	
k	0.30	0.35	0.40	

Figure 12 Au2001 Cross Sections

Note:

1. All Dimensions are in Millimeters (mm)

8 Ordering Information

Table 11 Ordering Information for Au2001

Ordering Part Number (OPN)	Marking	Package	Shipping Package	Temp. Range	MSL Level
Au2001B-QMR	AU2001B	16-Pin QFN 3 mm x 3 mm	Tape and Reel	–40 to 85 °C	MSL3

Notes:

1. Add an R at the end of the OPN to denote tape and reel ordering option.

The following figure gives an example of topside marking.

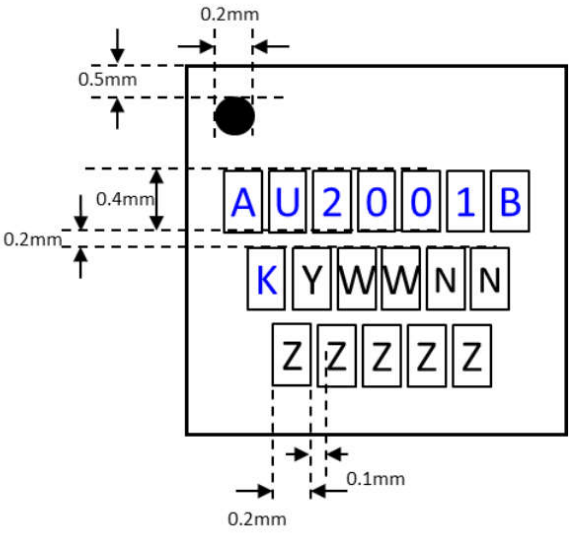


Figure 13 Au2001B Marking (package top view)

9 Revision History

Table 12 Revision History

Version Number	Date	Description	Author
0.1	1st October 2019	Document Created	AuraSemi
0.2	8th October 2020	Removed some text not relevant. Updated current numbers	AuraSemi
0.3	20th July 2021	1. Updated the description. 2. Updated current consumption value. 3. Removed some text not relevant.	AuraSemi
0.4	12th August 2021	Updated current consumption value.	AuraSemi
0.5	17th April 2022	1. Added applications. 2. Updated the logo. 3. Add package Information and ordering Information. 4. Modify the recommended voltage range.	AuraSemi

10 Trademarks

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11 Contact Information

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