Au8010A: Low Noise 1A LDO Datasheet

General Description

The Au8010A is a low-noise (6 μVRMS), low-dropout linear regulator (LDO) capable of sourcing 1A with only 75mV(max) of dropout. The device output voltage is adjustable from 0.8 V to 6 V using an external resistor divider.

Au8010A is the ideal choice to power noise-sensitive components found in high speed interfaces such as SERDES, communication infrastructure such as High Speed ADCs, DACs and RF components due to its exceptional PSRR and low noise (6 μVRMS) characteristics.

The 5V output capability of this device is well suited for RF amplifiers and RF front end. The Au8010A device is also well suited for digital loads such as ASICs, FPGAs, and DSPs that require a low-input voltage and low-output voltage to minimize power dissipation while providing excellent transient performance that caters to current steps in digital loads due to clock domain switching, dynamic power and frequency scaling. The soft-start capability minimizes in-rush current, thereby allowing for a smooth and reliable start-up at the system level.

Features

- Low Dropout: 75 mV max at 1 A
- 1.5% (max) Accuracy Over Line, Load, and Temperature
- Output Voltage Noise:6 μVRMS at 0.8 V Output
- Input Voltage Range:2.2 V to 6.5 V
- Output Voltage Range:0.8 V to 6 V (Set by resistor divider)
- Excellent PSRR of 38 dB at 1MHz, 57dB at 100kHz
- Stable with low ESR ceramic capacitor.
- Excellent Load Transient Response
- Adjustable Soft-Start In-Rush Control
- 3 mm × 3 mm, 8-Pin DFN

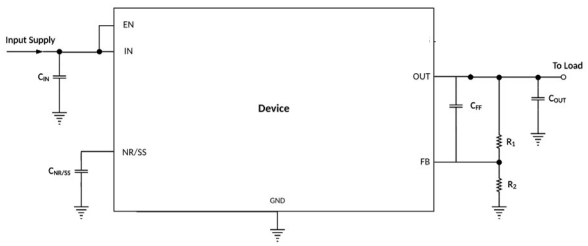

Figure 1 Typical Application Schematic

Applications

- Telecom MIMO RF front end components
- Digital Loads: SerDes, FPGAs and DSPs
- High-speed Analog Circuits:
    - VCO, ADC, DAC, and LVDS

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1 Pin Configuration

1.1 Pin Configuration Diagram

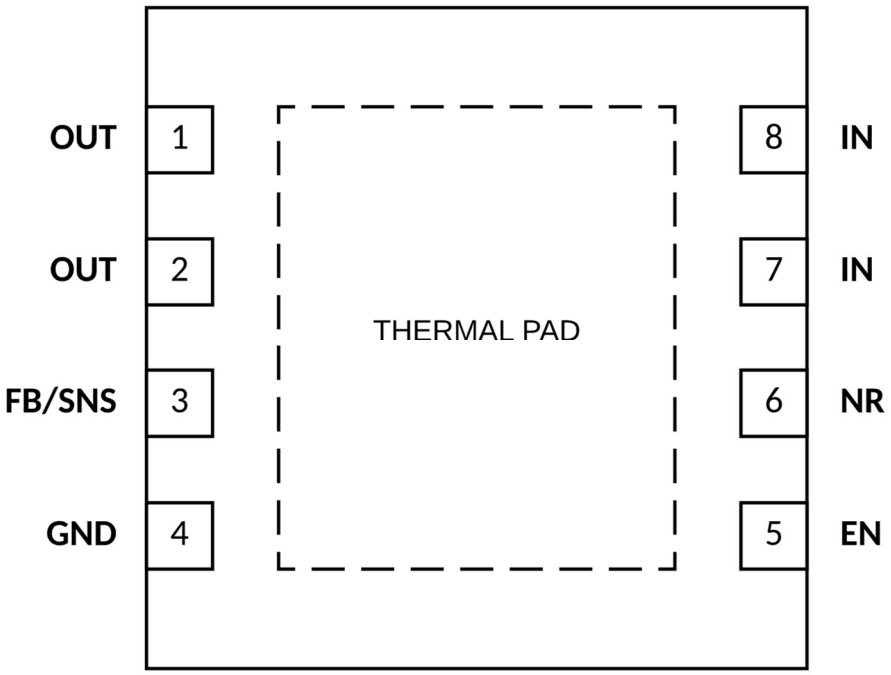


Figure 2 Au8010A Pin Configuration

1.2 Pin Description

Table 1 Pin Functions

Pin Name	Pin No.	I/O	Description
OUT	1,2	O	Regulated output pin. A 4.7 μF (Effective Capacitance) or larger ceramic capacitor from OUT to ground is required for stability and must be placed as close to the output as possible. Minimize the impedance from the OUT pin to the load.
FB/SNS	3	I	Feedback pin connected to the error amplifier. Although not required, a 10 nF feed-forward capacitor from FB to OUT (as close to the device as possible) is recommended to maximize AC and noise performance.
GND	4	—	Ground pin. This pin must be connected to ground with a low-impedance connection.
EN	5	I	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. If enable functionality is not required, this pin must be connected to IN.
NR	6	—	Noise-reduction and soft-start pin. Connecting an external capacitor between this pin and ground reduces reference voltage noise and also enables the soft-start function. Although not required, a 10 nF or larger capacitor is recommended to be connected from NR/SS to GND (as close to the pin as possible) to maximize ac performance.
IN	7,8	I	Input supply voltage pin. A 10 μF or larger ceramic capacitor from VIN to ground is recommended to reduce the impedance of the input supply. Place the input capacitor as close to the input as possible.
Thermal pad		—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

2 Electrical Specifications

Table 2 Absolute Maximum Ratings

Over junction temperature range (unless otherwise noted) [1]

Parameter	Pin	Min	Max	Units
Voltage	IN, PG, EN	–0.3	7.0	V
	SNS, OUT	–0.3	V_{IN} +0.3 [2]	V
	NR/SS, FB	–0.3	3.6	V
Current	OUT	Internally limited		A
	PG (sink current into device)		5	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{STG}		–55	150	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 4 . Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The absolute maximum rating is VIN +0.3 V or 7.0 V, whichever is smaller.

Table 3 ESD Ratings

Parameter	Conditions	Symbols	Value	Units
Electro Static Discharge	Human Body Model	V_{ESD}	±2000	V
	Charged Body Model		±500	

Table 4 Recommended Operating Conditions

Over junction temperature range (unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input supply voltage range	V_{IN}	2.2		6.5	V
Output voltage range [1]	V_{OUT}	0.8		6	V
Enable voltage range	V_{EN}	0		V_{IN}	V
Output current	I_{OUT}	0		1	A
Input capacitor	C_{IN}	10			µF
Output capacitor	C_{OUT}	4.7		100	µF
Power-good pullup resistance	R_{PG}	10		100	kΩ
NR/SS capacitor	$C_{NR/SS}$		10		nF
Feed-forward capacitor	C_{FF}		10		nF
Operating junction temperature	T_J	–40		125	°C

Notes:

1. This output voltage range does not include device accuracy or accuracy of the feedback resistors.

Table 5 Thermal Information

THERMAL METRIC	Symbol	Au8010A QFN 8 PINS	UNIT
Junction-to-ambient thermal resistance	$R_{\theta JA}$	48	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$	23	°C/W

Table 6 Electrical Specifications

Over operating junction temperature range (T_J = –40 °C to +125 °C), V_{IN} = 2.2 V or V_{IN} = $V_{OUT(nom)}$ + 0.4 V (whichever is greater), $V_{OUT(nom)}$ = 0.8 V [1], V_{EN} = 2.2 V, C_{IN} = 10 µF, C_{OUT} = 4.7 µF, $C_{NR/SS}$ without C_{FF}, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted. Typical values are at T_J = 25 °C.

Parameter	Condition	Symbol	Min	Typ	Max	Units
Input supply voltage range [2]		V_{IN}	2.2		6.5	V
Feedback voltage		V_{FB}		0.8		V
NR/SS pin voltage		$V_{NR/SS}$		0.8		V
Input supply UVLO	V_{IN} rising	$V_{UVLO(IN)}$	1.86	2	2.1	V

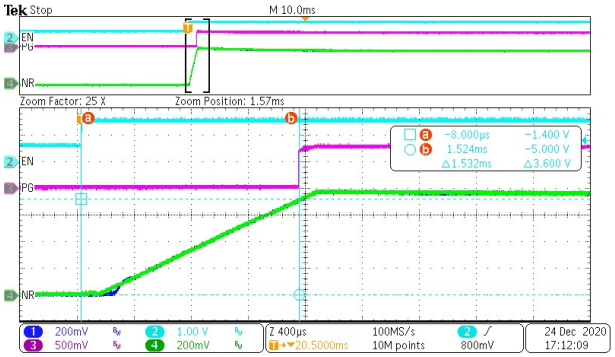
Parameter		Condition	Symbol	Min	Typ	Max	Units
$V_{UVLO1(IN)}$ hysteresis			$V_{HYS(IN)}$		200		mV
Output Voltage	Range		V_{OUT}	0.8-1.5%		6+1.5%	V
	Accuracy			-1.5%		1.5%	%
Line regulation		I_{OUT} = 5 mA, 2.2 V ≤ V_{IN} ≤ 6.5 V	ΔV_{OUT} / ΔV_{IN}		0.01		mV/V
Load regulation		5 mA ≤ I_{OUT} ≤ 1 A	ΔV_{OUT} / ΔI_{OUT}		0.08		mV/A
Dropout voltage		V_{IN} = 2.2 V, I_{OUT} = 1 A, V_{FB} = 0.8 V	V_{DO}			75	mV
Output current limit		V_{OUT} forced at 0.9 × $V_{OUT(nom)}$, V_{IN} = $V_{OUT(nom)}$ + 0.4 V	I_{LIM}	1.1		1.25	A
GND pin current		V_{IN} = 6.5 V, I_{OUT} = 5 mA	I_{GND}		2		mA
		V_{IN} = 2.2 V, I_{OUT} = 1 A			2.4		mA
		Shutdown, PG=open, V_{IN} = 6.5 V, V_{EN}=0.5V			1.2	25	μA
EN pin current		V_{IN} = 6.5 V, V_{EN} = 0 V and 6.5 V	I_{EN}	-0.1		0.1	μA
EN pin low-level input voltage (disable device)			$V_{IL(EN)}$	0		0.5	V
EN pin high-level input voltage (enable device)			$V_{IH(EN)}$	1.1		6.5	V
Soft start time		$V_{OUT(NOM)}$ = 3.3 V, V_{OUT} = 0%–90% $V_{OUT(NOM)}$, R_L = 3.3 kΩ, C_{OUT} = 4.7 μF	C_{NR} = 10 nF		1.6		ms
FB pin leakage current		V_{IN} = 6.5 V	I_{FB}	–100		100	nA
Power supply ripple rejection		V_{IN} – V_{OUT} = 0.4 V, I_{OUT} = 1 A, $C_{NR/SS}$ = 10 nF, C_{OUT} = 4.7μF F = 100 kHz, V_{OUT} = 5.0 V	PSRR		57		dB
		V_{IN} – V_{OUT} = 0.4 V, I_{OUT} = 1 A, $C_{NR/SS}$ = 10 nF, C_{OUT} = 4.7μF F = 500kHz, V_{OUT} = 5.0 V			34		dB
		V_{IN} – V_{OUT} = 0.4 V, I_{OUT} = 1 A, $C_{NR/SS}$ = 10 nF, C_{OUT} = 4.7μF F = 1MHz, V_{OUT} = 5.0 V			38		dB
Output noise voltage		BW = 10Hz to 100 kHz, V_{IN} = 2.2 V, V_{OUT} = 0.8 V, I_{OUT} = 1 A, $C_{NR/SS}$ = 100 nF, C_{OUT} = 4.7 μF	V_N		6		μV_{RMS}
Thermal shutdown temperature		Shutdown, temperature increasing	T_{SD}		150		°C
		Reset, temperature decreasing			130		°C

Notes:
1. VOUT(nom) is the expected VOUT value set by the external feedback resistors.
2. When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.
3. The device is not tested under conditions where V_{IN} > V_{OUT} + 1.7 V and I_{OUT} = 1 A, because the power dissipation is higher than the maximum rating of the package.

3 Typical Characteristics

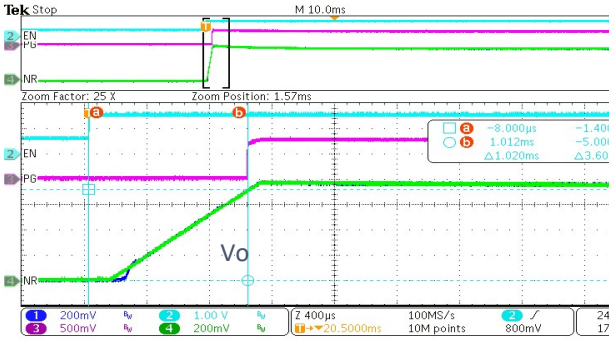
At VOUT(TYP) = 3.3 V, VIN = VOUT(TYP) + 0.4 V or 2.2 V (whichever is greater), IOUT = 1 A, VEN = VIN, CIN = 10 µF, COUT = 4.7 µF, and CNR = 0.01 µF, all temperature values refer to TJ (unless otherwise noted).

Power On from EN



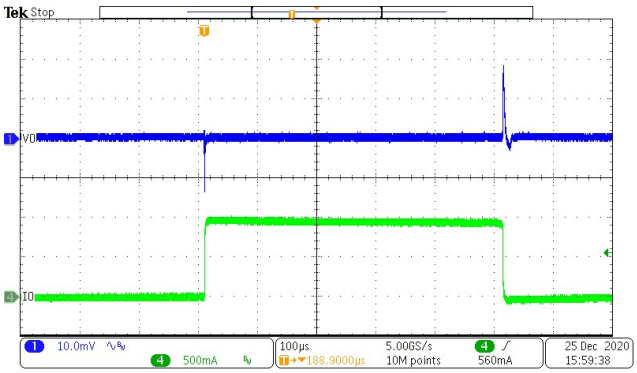
Vin=6.5v,Io=5mA,EN to PG=1.53ms. CNRSS=1nF.

Power on from EN with Iload



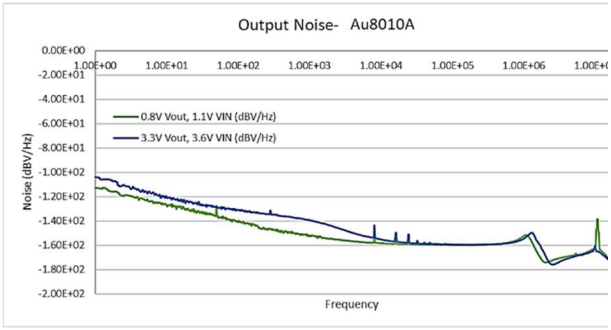
Vin=6.5v,Io=1A,EN to PG=1ms. CNRSS=1nF.

Load Transient



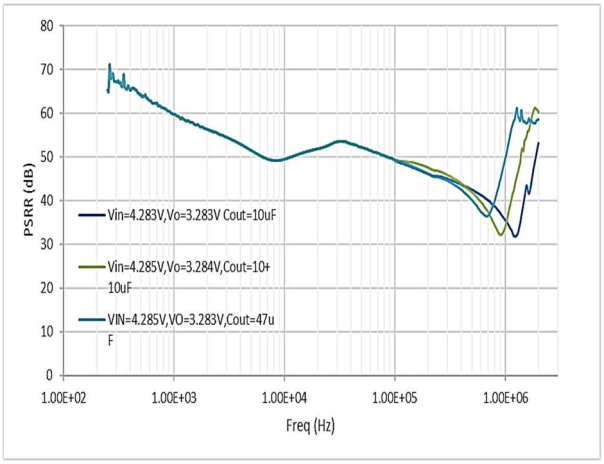
Vin=1.1V,Vo=0.8V,CNR=1nF,Cff=0,Cout=10uF(5mA->1A->5mA). Slew rate: 1A/us.

Noise

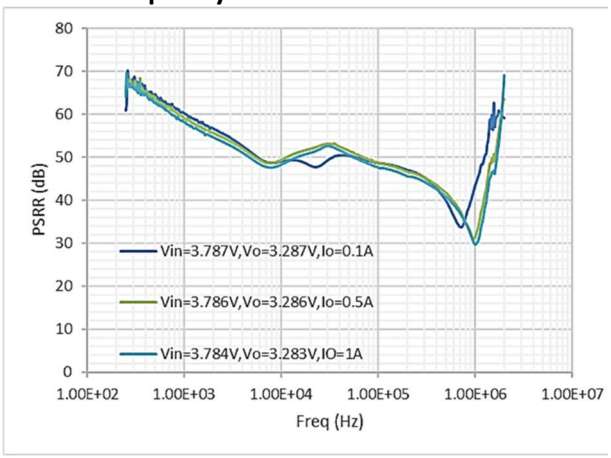


Conditions: Cout=10uF, Cnrss=100nF, Cff=10nF, Iout= 1A, VIN=Vout+0.3V

PSRR vs Cout



PSRR vs frequency and Iout



4 Detailed Description

4.1 Overview

The Au8010A is a high-current (1 A), low-noise (6 μV_{RMS}), high accuracy (1.5%) low-dropout linear voltage regulator (LDO). These features make the device a robust solution to solve many challenging problems in generating a clean, accurate power supply.

The Au8010A has several features that make the device useful in a variety of applications. As detailed in the Functional Block Diagram section, these features include:

- Low-noise, high-PSRR output
- Programmable soft-start
- Enable circuitry
- Thermal protection

Overall, these features make the Au8010A the component of choice because of its versatility and ability to generate a supply for most applications.

4.2 Functional Block Diagram

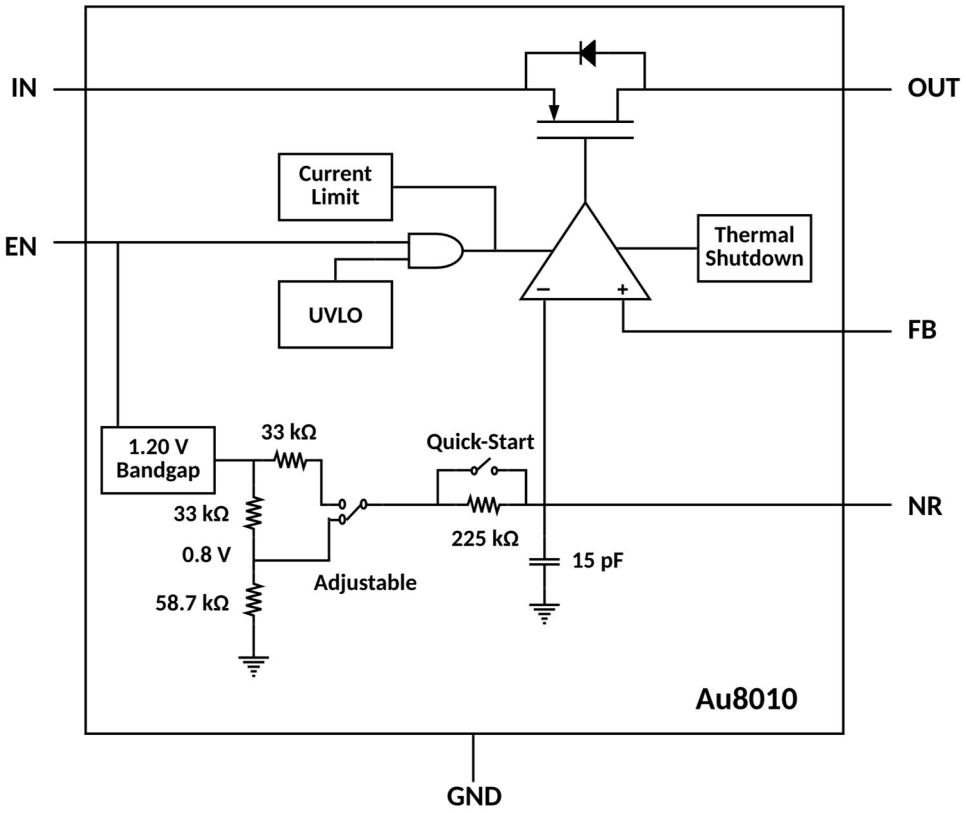


Figure 3 Functional Block Diagram Adjustable Voltage

4.3 Feature Description

4.3.1 Programmable Soft-Start

Soft-start refers to the ramp-up time of the output voltage during LDO turn-on after EN and UVLO exceed the respective threshold voltage. The noise-reduction capacitor ($C_{NR/SS}$) serves a dual purpose of both governing output noise reduction and programming the soft-start ramp time during turn-on. The start up ramp is monotonic and linear in most conditions, however there is a small set of conditions that cause a small initial jump in output voltage.

4.3.2 Internal Current Limit (ILIM)

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. During a current-limit event, the LDO sources constant current; therefore, the output voltage falls with decreased load impedance. Thermal shutdown can activate during a current limit event because of the high-power dissipation typically found in these conditions. To ensure proper operation of the current limit, minimize the inductances to the input and load. Continuous operation in current limit is not recommended.

4.3.3 Enable

The enable pin for the Au8010A is active high. The output of the Au8010A is turned on when the enable pin voltage is greater than its rising voltage threshold (1.1 V, max), and is turned off when the enable pin voltage is less than its falling voltage threshold (0.5 V, min). A voltage less than 0.5 V on the enable pin disables all internal circuits. At the next turn-on this voltage ensures a normal start up waveform with in rush control, provided there is enough time to discharge the output capacitance.

When the enable functionality is not desired, EN must be tied to V_{IN}.

4.3.4 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit monitors the input voltage (V_{IN}) to prevent the device from turning on before V_{IN} rises above the lockout voltage. The UVLO circuit also disables the output of the device when V_{IN} falls below the lockout voltage. The UVLO circuit responds quickly to glitches on V_{IN} and attempts to disable the output of the device if either of these rails collapse. As a result of the fast response time of the input supply UVLO circuit, fast and short line transients well below the input supply UVLO falling threshold can cause momentary glitches when asserted or when recovered from the transient.

4.3.5 Thermal Protection

The Au8010A contains a thermal shutdown protection circuit to disable the device when thermal junction temperature (T_J) of the main pass-FET exceeds 150°C (typical). Thermal shutdown hysteresis assures that the LDO resets again (turns on) when the temperature falls to 130°C (typical). The thermal time constant of the semiconductor die is fairly short, and thus the device cycles on and off when thermal shutdown is reached until the power dissipation is reduced. For reliable operation, limit the junction temperature to a maximum of 125 °C. Operation above 125 °C can cause the device to exceed its operational specifications. Although the internal protection circuitry of the Au8010A is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the Au8010A into thermal shutdown or above a junction temperature of 125 °C reduces long-term reliability.

4.4 Device Functional Modes

4.4.1 Operation with 2.2 V ≤ V_{IN} ≤ 6.5 V

If the input voltage is equal to or exceeds 2.2 V, the LDO is operational.

4.4.2 Shutdown

Shutting down the device reduces the ground current of the device to a maximum of 25 μA.

5 Application and Implementation

NOTE: Information in the following applications sections is not part of the Aura Semiconductor component specification, and Aura Semiconductor does not warrant its accuracy or completeness. Aura Semiconductor's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

5.1 Recommended Capacitor Types

The Au8010A is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin (NR, pin 6). Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature. As a rule of thumb, derate ceramic capacitors by at least 50%. The input and output capacitors recommended herein account for a capacitance derating of approximately 50%, but at high V_{IN} and V_{OUT} conditions (that is, V_{IN} = 5.5 V to V_{OUT} = 5.0 V) the derating can be greater than 50% and must be taken into consideration.

5.1.1 Input and Output Capacitor Requirements (C_{IN} and C_{OUT})

The Au8010A is designed and characterized for operation with ceramic capacitors with effective capacitance of 4.7 μF or greater at the output and 10 μF or greater (5 μF or greater of capacitance) at the input. Place the capacitors as close to the pins as possible to minimize ringing. Caps rated to 125 deg C are recommended.

5.1.2 Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)

The Au8010A features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor ($C_{NR/SS}$). The use of an external $C_{NR/SS}$ is highly recommended, especially to minimize in-rush current into the output capacitors. This soft-start eliminates power-up initialization problems when powering field-programmable processors. The controlled voltage ramp of the output also reduces peak in-rush current during start-up, minimizing start-up transients to the input power bus.

Soft-start ramp time can be calculated with Equation 1:

$$t_{SS} = 76000 \times C_{NR/SS} \quad (1)$$

The noise-reduction capacitor, in conjunction with the noise-reduction resistor, forms a low pass filter (LPF) that filters out the noise from the reference before being gained up with the error amplifier, thereby reducing the device noise floor. The LPF is a single-pole filter and the cutoff frequency can be calculated with Equation 2. The typical value of R_{NR} is 1 MΩ. Increasing the $C_{NR/SS}$ capacitor has a greater affect because the output voltage increases when the noise from the reference is gained up even more at higher output voltages. For low-noise applications, a 10 nF to 1 µF $C_{NR/SS}$ is recommended.

$$fcutoff = 1 / (2 \times \pi \times R_{NR} \times C_{NR/SS}) \quad (2)$$

5.1.3 Feed-Forward Capacitor (C_{FF})

Although a feed-forward capacitor (C_{FF}) from the FB pin to the OUT pin is not required to achieve stability, a 10 nF external feed-forward capacitor optimizes the transient, noise, and PSRR performance. A higher capacitance C_{FF} can be used; however, the start-up time is longer and the power-good signal can incorrectly indicate that the output voltage is settled.

5.1.4 Optimizing Noise and PSRR

The ultra-low noise floor and PSRR of the device can be improved by careful selection of:

- $C_{NR/SS}$ for the low-frequency range
- C_{FF} in the mid-band frequency range
- C_{OUT} for the high-frequency range
- V_{IN} - V_{OUT} for all frequencies, and

A larger noise-reduction capacitor improves low-frequency PSRR by filtering any noise coupling from the input into the reference. The feed-forward capacitor can be optimized to place a pole-zero pair near the edge of the loop bandwidth and push out the loop bandwidth, thus improving mid-band PSRR. Larger output capacitors and various output capacitors can be used to improve high-frequency PSRR.

5.1.5 Vout Selection

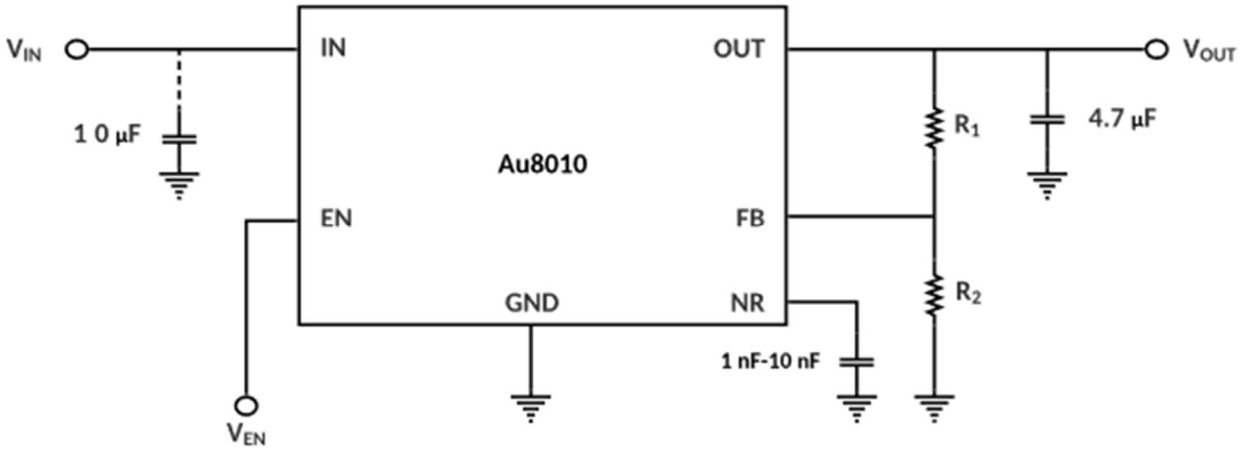


Figure 4 Typical Application Adjustable Voltage

R_1 and R_2 can be calculated for any output voltage range using Equation 3. This resistive network must provide a current equal to or greater than 5 µA for dc accuracy. Using an R1 of 12.1 kΩ is recommended to optimize the noise and PSRR.

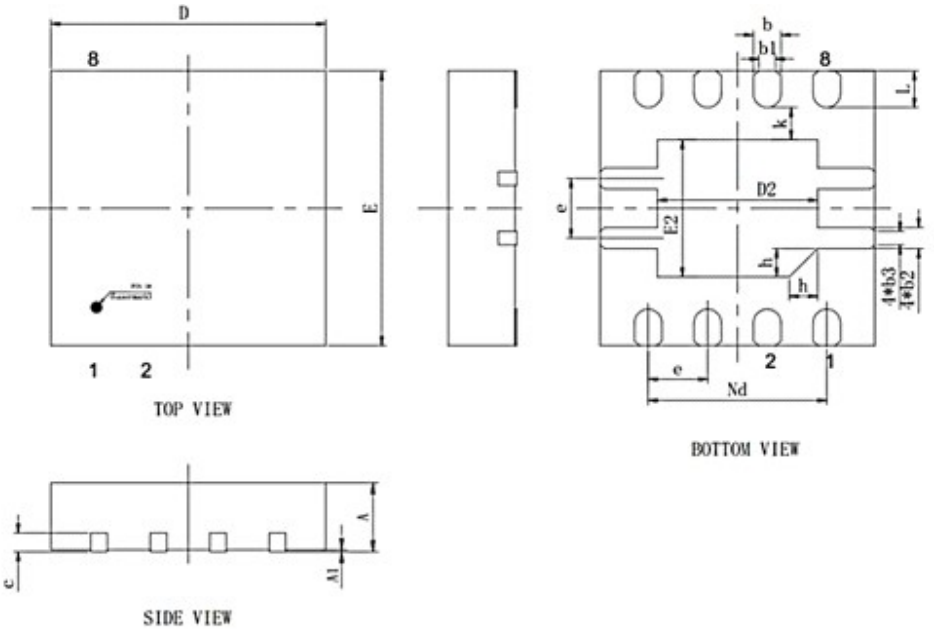
$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (3)$$

Table 7 shows the resistor combinations required to achieve several common rails using standard 1%-tolerance resistors.

Table 7 Recommended Feedback-Resistor Values

$V_{OUT(NOM)}$ (V)	Feedback Resistor Values	
	R_1 (kΩ)	R_2 (kΩ)
0.8V	0	DNP
1	2.49k	10k
1.2	4.99k	10k
1.5	8.87k	10k
1.8	12.5k	10k
2.5	21k	10k
3.3	30.9k	10k
5	52.3k	10k

6 Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.85	0.90	0.95
A1	0	0.02	0.05
b	0.25	0.30	0.35
b1	0.18REF		
b2	0.18	0.23	0.28
b3	0.15REF		
c	0.203REF		
D	2.90	3.00	3.10
D2	1.65	1.75	1.85
Nd	1.95BSC		
E	2.90	3.00	3.10
E2	1.40	1.50	1.60
e	0.65BSC		
K	0.35REF		
L	0.35	0.40	0.45
h	0.26	0.31	0.36

Figure 5 Package Dimensions

Tape and Reel Info:

Device	Package type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
Au8010BA-DNR	DFN 3X3	8	4000	330	12.3	3.3	3.3	1.1	8	12	Q2

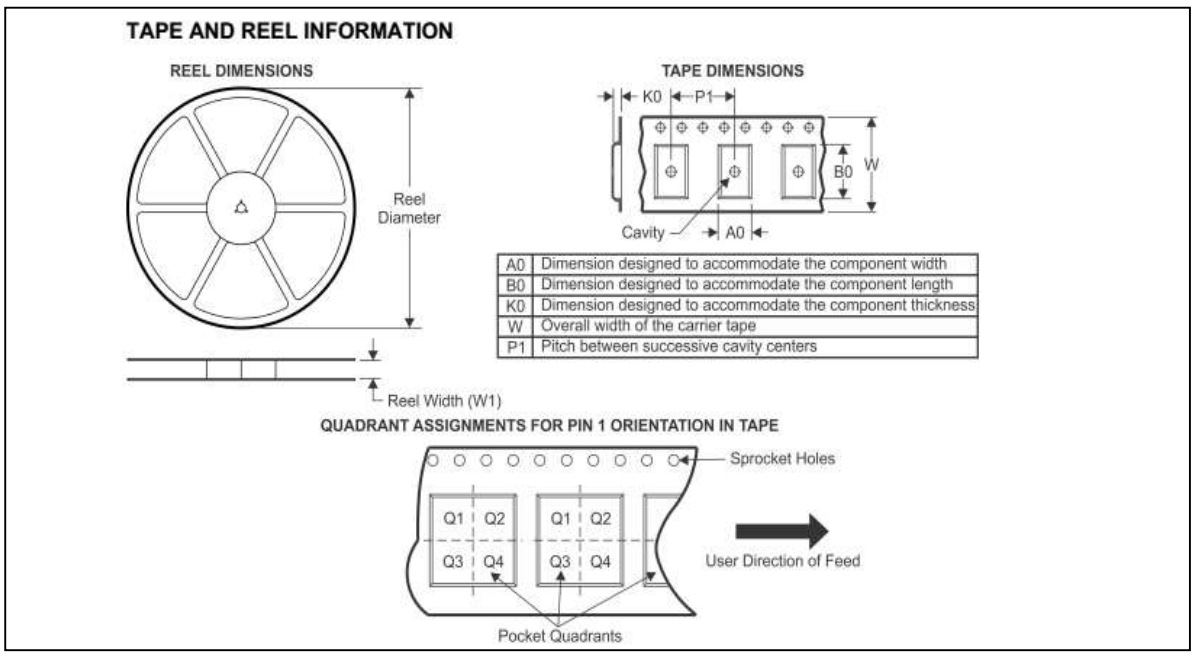


Figure 6 Tape and Reel Drawing

7 Ordering Information

Table 8 Ordering Information

Ordering Part Number (OPN)	Marking	Package	Shipping Package	Temperature Range	MSL Rating
Au8010BA-DNR	8010BA	8-Pin DFN	Tape and Reel	-40°C to 125°C	MSL2
Au8010BA-EVB			Evaluation Board		

Marking:

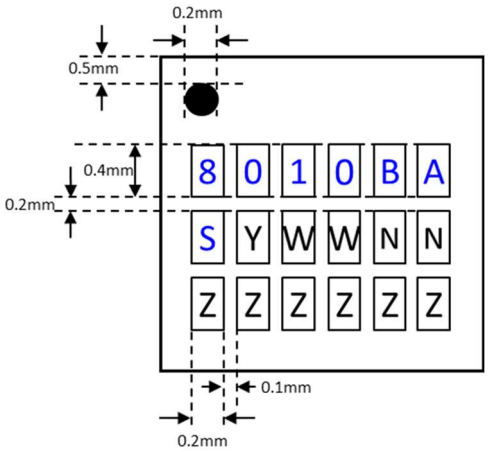


Figure 7 Package Marking

8 Revision History

Table 9 Revision History

Version Number	Date	Description	Author
1.0	21st Nov 2021	Document Created	AuraSemi
1.1	22nd April 2022	Added Tape and reel diagram, MSL rating and marking info	

9 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

10 Contact Information

For more information visit www.aurasemi.com
For sales related information please send an email to sales@aurasemi.com